

curamik®
ENABLING POWER EFFICIENCY

PACKAGING TECHNOLOGIES

SiC Chip Assembly on Substrate

- High precision & tilt-free assembly (+/- 10 µm in x/y/z)
- Sintering of prepackaged SiC chip on copper surface

Encapsulation

- Transfer molding technology
- Encapsulant suitable for subsequent via lasering
- Encapsulation of thick substrate (4.5 mm) with challenging filling geometry

Redistribution & SiC Interconnection

- Direct metallization of molding surface
- Laser drilling of blind vias in epoxy molding compound (400 µm / 1000 µm)
- Surface finish according to subsequent SMD assembly

SMD Assembly

- State-of-the-art lead-free soldering of SMDs

For further information please go to
www.izm.fraunhofer.de/bernstein

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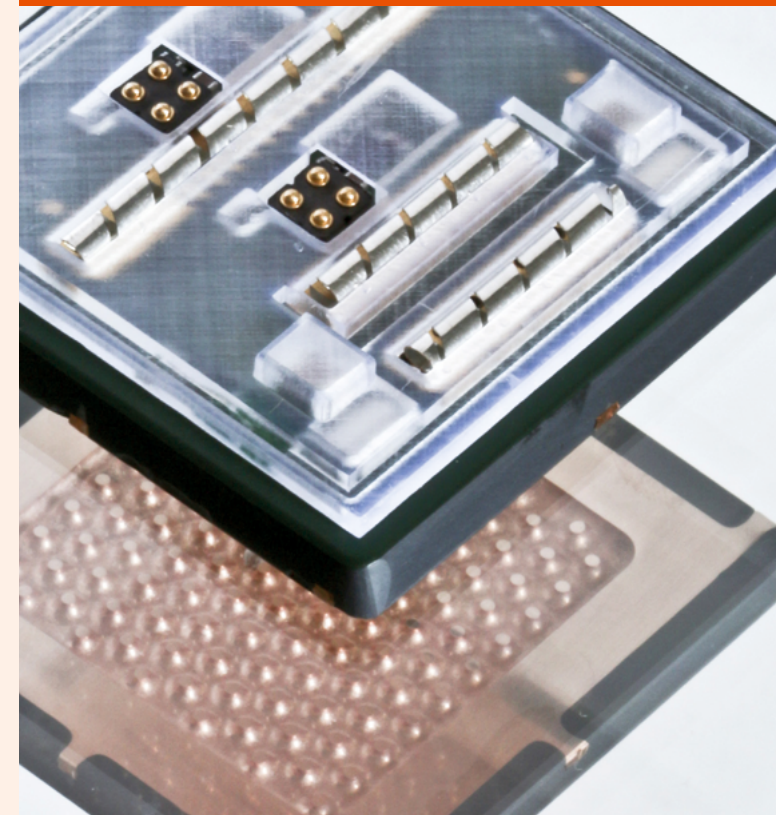
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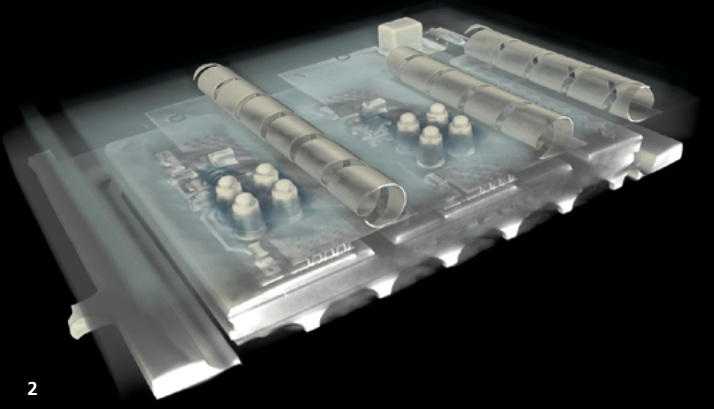
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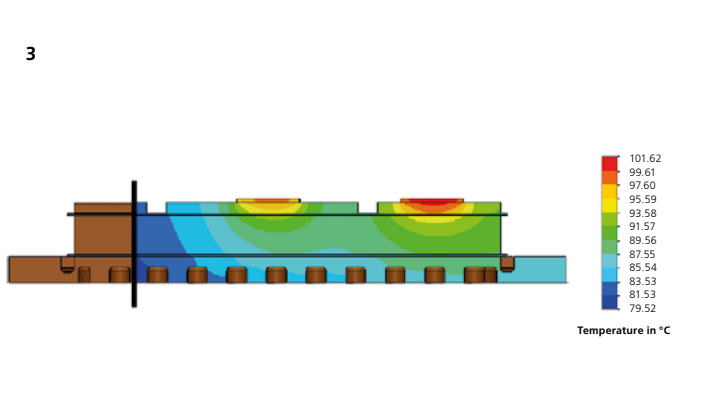
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ULTRA LOW INDUCTIVE MULTI- LAYER CERAMIC SiC POWER MODULE

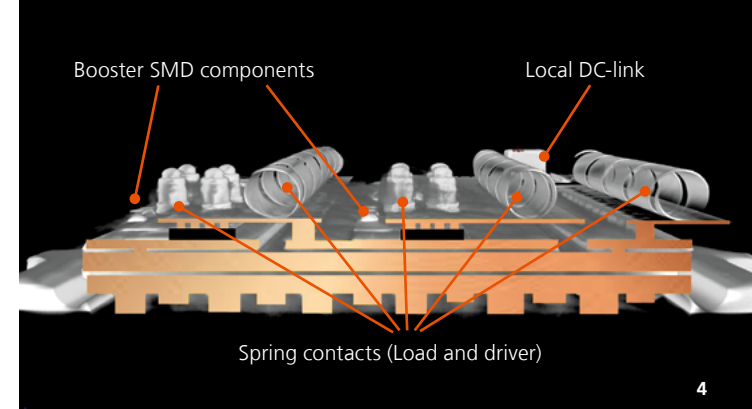




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APPLICATIONS

To make use of the superior properties of Wide Band Gap (WBG) semiconductors power modules are needed with optimized parasitic electromagnetic properties and high temperature capability, furthermore with the possibility for a high degree of integration:

Requirements on Wide Band Gap power modules:

- Low inductive commutation cell,
- Low inductive gate path,
- Low inductive input connectors,
- Very low thermal resistance.

Advanced low inductive power modules provide unique features such as:

- Lowest possible switching losses,
- A low $R_{ds,on}$,
- Nearly no voltage overshoot while turn-off,
- More output power out of the same chip,
- Reduction in size and weight.

Thus, they are interesting for a wide range of automotive, solar energy and industrial applications.

Cover Power System in Package (PSiP) in mold technology

1 curamik® multilayer ceramic substrate with integrated heatsink supplied by Rogers Corporation and sintered prepackages

2 X-ray-CT screening of the molded power module

3 Fluid dynamic thermal simulation, $P_{L,chip} = 50\text{ W}$, $T_{fluid} = 75^\circ\text{C}$

4 Side view of the Power System in Package (PSiP) in mold technology

POWER MODULE DESIGN

This ultra-compact low inductive power module design contains many innovations, which allow a high power density combined with an excellent electrical performance.

The basis forms a curamik® multilayer ceramic substrate supplied by Rogers Corporation with two electrical layers on top and in the middle. The insulated bottom copper layer contains an integrated heat sink. In spite of two ceramic layers a very low thermal resistance below 0.265 K/W from junction to fluid can be reached.

After sintering the SiC MOSFETs onto the ceramic substrate the assembly is molded. On top of the mold cap a structured electrical copper layer is implemented and electrically connected to the substrate with drilled blind vias. The combination of the innovative substrate, the additional electrical layer on the mold cap and thus the integration of a local DC-Link on-board offer a very low inductive commutation cell design with $L_\sigma < 2\text{ nH}$.

It also allows for a very low inductive DC+/- input connection, an implementation of SMD components and consequently a first on-board driver stage with lowest parasitic stray inductance in the gate path to the chip.

TECHNICAL DATA

Electrical characteristics

- Half bridge design
- $U_{ds,max} = 1200\text{ V}$
- $R_{ds,on} = 11\text{ m}\Omega$
- $I_{out,eff} = 160\text{ A}$
- Power range up to 50 kW (150 kW for 3 phases)
- Local DC-Link on-board
- SMD components on-board
- Driver booster on-board for lowest gate inductance
- $L_{\sigma, power module} < 2\text{ nH}$

Thermal characteristics

- Integrated heatsink in the ceramic substrate
- Insulated heatsink
- Single sided cooling
- $R_{th(junction-fluid)} \leq 0.265\text{ K/W}$

Mechanical characteristics

- Ultra-compact design
- Size: 48 mm x 48 mm x 5 mm + SMD components and frame
- Multilayer Si_3N_4 ceramic substrate
- Spring contacts (Load and driver)